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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	Examiner	Group Art Unit	

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☑ Responsive to communication(s) filed on 01/04/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-15 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☑ Claim(s) 1-15 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s).____ ☐ Interview Summary, PTO-413

☑ Notice of References Cited, PTO-892 ☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Other____

Office Action Summary

DETAILED ACTION

1. Claims 1-~~15~~ 22 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-4 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Rajski et al.** (Rajski) patent no. **5,991,898**, in view of **Chandra et al.** (Chandra) patent no. **5,206,862**.

As per claims 1 and 10:

Rajski teaches the invention substantially as claimed, including an integrated circuit [IC 10, Fig. 1] having logic blocks [CUT 14, Fig. 1] comprising:

a control unit [embedded processor core 12, Fig. 1] for performing test and debug operations of said logic blocks of said integrated circuit;

a memory [non-volatile memory 18, Fig. 1] associated with said control unit, said memory holding instructions for said control unit [col. 5 lines 50-60]; and

a plurality of scan lines [scan registers 16, Fig. 1] responsive to said control unit for loading test signals for said logic blocks and retrieving test signal results from said logic blocks, said test

signals and said test signal results stored in said memory so that said loading and retrieving operations are performed to said integrated circuit [col. 4 lines 23-42].

Rajski does not teach a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points.

Chandra teaches an integrated circuit having comprising a control unit [test point array 14, Fig. 1], a memory [instruction register 20, Fig. 1], and a plurality of probe lines responsive to said control unit for carrying system operation signals at predetermined probe points of said logic blocks [col. 3 lines 30-40].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Rajski to provide a built in self test of multiple scan based integrated having plurality of probe lines for carrying system operation signals at predetermined probe points as taught by Chandra. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide test signals to select test points while response are sensed [see Chandra, col. 1 lines 37-47].

As per claim 3:

Rajski teaches the integrated circuit further comprising a unit [data path 12, Fig. 5] coupled to said control unit and said memory, said unit testing said logic blocks and said memory responsive to and in cooperation with said control unit to self-test said integrated circuit.

As per claim 4:

Rajski teaches the integrated circuit wherein said scan lines comprise a first string of flip-flop [LFSR 50, Fig. 7] connectors connected between logic block and the remainder of said integrated

circuit proximate said logic block [scan registers 16 connected between blocks CUT, Fig. 1], said flip-flop connectors providing signal paths between said logic block and the remainder of said integrated circuit proximate said logic block in one mode and carrying test signals and test signal results in a second mode [test mode 21, Fig. 2, claim 25, col. 19 begin at line 9].

4. Claims 2, 5-9 and 15-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Rajski et al.** (Rajski) patent no. **5,991,898**, in view of **Chandra et al.** (Chandra) patent no. **5,206,862**, and further in view of **Mori** patent no. **6,003,142**.

As per claim 2:

Rajski and Chandra do not teach loading and retrieving operations are performed at one or more clock signal rates internal to said integrated.

Mori teaches a test facilitating circuit of microprocessor including loading and retrieving operations performing at one or more clock signal rates internal to said integrated circuit [see signal INTERNAL CLOCK of Fig. 6A-B, col. 2 lines 26-53 and col. 3 lines 10-28].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski and Chandra to include a facilitating circuit as taught by Mori for loading and retrieving operations at one or more clock signal rates internal to integrated circuit. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide an efficient method of testing a high frequency integrated circuit using an inexpensive tester [see Mori col. 1 lines 6-11 and col. 1 line 61 - col. 2 line 10].

As per claim 5:

Mori teaches the integrated circuit wherein said scan lines [JTAG boundary scan 17, Fig. 3] comprise a second string of flip-flop connectors [shift register 16, Fig. 3] between elements of a logic block, said flip-flop connectors providing signal paths between said logic block elements in one mode and carrying test signals and test signal results in a second mode [col. 2 lines 16-68].

As per claims 6-9:

Chandra teaches probes lines comprises a string of programmable connectors providing a signal path for carrying system operation signal at predetermined probe points of said logic blocks [Fig. 2].

As per claim 15:

Rajski and Chandra teaches the invention substantially as claimed as discussed in claim 1 above. However, Rajski and Chandra do not teach loading and retrieving operations are performed at one or more clock signal rates internal to said integrated.

Mori teaches a test facilitating circuit of microprocessor including loading and retrieving operations performing at one or more clock signal rates internal to said integrated circuit [see signal INTERNAL CLOCK of Fig. 6A-B, col. 2 lines 26-53 and col. 3 lines 10-28].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski and Chandra to include a facilitating circuit as taught by Mori for loading and retrieving operations at one or more clock signal rates internal to integrated circuit. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide an efficient method of testing a high

frequency integrated circuit using an inexpensive tester [see Mori col. 1 lines 6-11 and col. 1 line 61 - col. 2 line 10].

loading said scan lines responsive to said control unit with said test signals for said logic blocks [col. 4 lines 32-42];

retrieving test signal results from said logic blocks along said scan lines [col. 4 lines 32-42],

storing said test signal results in said memory [col. 5 lines 50-60]; and

processing [col. 6 lines 42-68, Fig. 2] said stored test results signals in said control unit responsive to said stored instructions in said memory to perform test and debug operations of said logic blocks of said integrated circuit.

Rajski does not teaches loading, retrieving and storing operations are performed at one or more clock signal rates internal to said integrated circuit.

Mori, in an analogous art, teaches a test facilitating circuit of microprocessor [see Fig. 3] including a control circuit 12 and a cache memory 1 wherein the loading, retrieving and storing operations are performed at one or more clock signal rates internal to said integrated circuit [see signal INTERNAL CLOCK of Fig. 6A-B]. After the test, an external tester reads the test results out of the cache memory and examines them [see col. 2 lines 26-53 and col. 3 lines 10-28].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teachings of Rajski to provide a built in self test circuitry including a facilitating circuit taught by Mori for loading, retrieving and storing operations at one or more clock signal rates internal to Rajski's integrated circuit because it would provide an efficient method of testing a high

frequency integrated circuit using an inexpensive tester [see Mori col. 1 lines 6-11 and col. 1 line 61 - col. 2 line 10].

5. Claims 11-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over **Rajski et al.** (Rajski) patent no. **5,991,898**, in view of **Chandra et al.** (Chandra) patent no. **5,206,862** and further in view of **Gheewala et al.** (Gheewala) patent no. **5,202,624**.

As per claims 11 and 12:

Rajski and Chandra do not teach an IC including a trigger logic.

Gheewala teaches a trigger logic [see circuitry of Fig. 3 and the logic of TABLE A on col. 6 and TABLE B on col. 8] responsive to said system operation signals for initiating/terminating storage of said system operation signals in said memory [when P1=0 and P2=0, S2 value is written into latch 68, when control signal C=1, the value then transmitted to driver 42, col. 7 lines 1-15].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Rajski and Chandra to include a trigger logic for initiating/terminating storage of said system operation signals in said memory as taught by Gheewala because it would provide the advantages that the test signals are loaded to internal probe points without the need for complex scan registers [see Gheewala col. 2 lines 42-57].

As per claim 13:

Gheewala teaches each of said probe lines comprises a string of programmable connectors [Fig. 3] providing a signal path for carrying system operation signals at predetermined probe points of said logic blocks in one mode [col. 2 lines 42-63].

As per claim 14:

Gheewala teaches each programmable connector of said probe lines is programmed by a flip-flop connector [latch 68, Fig. 3, col. 2 lines 13-22], each flip-flop connector connected between elements of said integrated circuit and forming part of string of flip-flop connectors, said flip-flop connectors providing signal paths between said integrated circuit elements in one mode and carrying signals for programming said programmable connectors in a second mode [col. 7 lines 1-15].

Response to Arguments

6. Applicant argues that the prior art of record do not teach the execution of normal operation of the integrated circuit while observing the probe points in operation.

The newly cited art, Chandra, teaches the execution of normal operation of the integrated circuit while observing the probe points in operation [col. 3 lines 30-40]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Chandra with the teachings of Rajski, Mori and Gheewala to provide a built in self test of multiple scan based integrated having plurality of probe lines for carrying system operation signals at predetermined probe points as taught by Chandra. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so because it would provide test signals to select test points while response are sensed [see Chandra, col. 1 lines 37-47].

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to (703) 308-6296

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

David Ton

Patent Examiner

April 02, 2001